IN THE SPECIFICATION

Please replace paragraph [0005] with the following amended paragraph:

[0005] In the first conventional technology described above, critical defects cannot be evaluated until the semiconductor device is completed and the testing process is reached. As a result, there is a delay between the time when a defect is generated and the time when ~~measures against ftirther~~ further defects can be ~~taken~~measured, making production of faulty products unavoidable. If critical defects are repeatedly generated at the same place on wafers, the coordinates obtained from inspections at intermediate processes can be used to detect generation of critical defects[[, but]]. However, this applies only to these restricted cases.

Please replace paragraph [0028] with the following amended paragraph:

[0028} Fig. 1 is a block diagram showing a defect analysis system relating to a first embodiment of the present invention. As the figure shows, the defect analysis system of this embodiment includes an inspection device 100, a review device 101, an electronic tester 102, a defect data management server 103, a classifying device 111, and a network 104 connecting these elements. ~~This figure~~Fig. 1 shows one example implementation of this invention, but it would also be possible to have, for example, the classifying device 111 equipped with the functions of a display device 109, an input device 110, and a storage device 108. [[Also]]In addition, the classifying device 111 ~~itself~~ may also be formed as a part of the defect

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data management server 103, the ~~detection~~ inspection device 100, or the review device 101.

Please replace paragraph [0029] with the following amended paragraph:

[0029] The flow of operations performed by the architecture shown in Fig. 1 will be described, with reference to Fig. 2. First, the inspection device 100 is used to perform a defect inspection of the wafer. When this inspection is completed, the review device 101 retrieves defect images 211 corresponding to defect coordinates 210 obtained from the defect inspection results and indicating positions of defects on the wafer. The associations between the images and the coordinates are stored in the storage device 108 by way of the defect data management server 103. Next, the electronic tester 102 performs an electronic test of the same wafer and determines fault coordinates 212 from the test. The defect data management

B3 server 103 performs a consistency check 213 between the defect coordinates 210 and the electronic testing fault coordinates 212. This operation allows the defect coordinates 210 to be classified into critical defects 214, which match the electronic test fault coordinates 212, and noncritical defects 215, which do not match. By using the associations between defect coordinates 210 and the defect images 211, the defect ~~defects~~ images 211 can be classified a critical defects 214 group and a non-critical defects 215 group. Based on the results of this classification and using the defect images belonging to the critical defects 214 and the noncritical defects 215, the classification device 111 obtains training data 216, in which image characteristics are quantified. This training data 216 has a high correlation with the electronic test results. Furthermore, the classification device 111 can generate learned data 217,

which contains parameters for converting image characteristics into categories, based on the training data 216. This would allow an unknown image 218 detected by a different wafer defect inspection to be classified accurately into the critical defects 214 group or the non-critical defects 215 group.

Please replace paragraph [0041] with the following amended paragraph:

[0041] The operations of the classifying device 111 will be described. A program installed in the classifying device 111 uses a known pattern recognition method such ~~s the one~~as described in "Image Analysis Handbook" (Takaki, et al., Tokyo Daigaku Shuppankai, 1991, pp. 171-205, pp. 641-688). In this pattern recognition method, characteristics of a sample image set up beforehand are compared with the characteristics of an unknown image. The unknown image is classified based on similarities of characteristics. Using a defect image as an example, the characteristics can be numerical data relating to defect color (including brightness), size, and shape.

Please replace paragraph [0045] with the following amended paragraph:

[0045] Fig. 3 shows an example in which the present invention is used in a semiconductor device production process. The defect analysis method of the present invention involves a preparation step using a wafer A 121 and an active step using a wafer B 122. The wafer A [[1221]]121 and the wafer B 122 refer to the use of distinct wafers rather than two specific wafers. In the preparation step, it would be desirable to use a small number of wafers A 121 while collecting as large a number of defect samples as possible. Thus, it would be preferable to use multiple wafers

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rather than just one. Also, it would be preferable to have these multiple wafers drawn from separate lots. Also, the wafers A and the wafers B can be of different types as long they are produced using similar processes.

Please replace paragraph [0073] with the following amended paragraph:

[0073] In addition to aluminum wiring processes, the following description will apply in a ~~smflar~~ similar manner to wiring production processes such as gate wiring. In Fig. 7 (b), critical and non-critical defects are classified by manually estimating electronic criticality from the image characteristics. The classification is performed by having the operator observe the images on the display device 109, visually evaluate criticality/non-criticality, and operate the input device 110.

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Please replace paragraph [0075] with the following amended paragraph:

[0075] Fig. 7 (c) shows displayed images of the results of the coordinate consistency checking initiated by clicking on a coordinate consistency checking button 224 on the display screen 1091 in Fig. 8. If the test result from the consistency data in Fig. 6 is 'G', the ~~defcdt~~ defect image is displayed as a noncritical defect. If the test result is 'N', the defect image is displayed as a critical defect.

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Please replace paragraph [0080] with the following amended paragraph:

[0080] Furthermore, by analyzing the image characteristics in each of the categories, an estimation of the causes of the defects can be made, as shown in Figs. 9(a) to 9(c), which show a cross-section of the defects from Fig. 7(c). The

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prominently projected contaminant is dark since it scatters the illuminating light more. The shorter contaminants scatter ~~hght~~ light to a lesser degree and therefore result in lighter images.

Please replace paragraph [0093] with the following amended paragraph:

[0093] The operation is ~~perfonnedin~~ performed in three steps: (a) a defect classification operation; (b) a coordinate consistency checking operation; and (c) a criticality calculation operation. In the defect classification operation (a), the defect data management server 103 from Fig. 1 reads into memory a defect map and an associated defect image stored in the storage device 108. The classification device 111 classifies the defect image and stores the classification results as electronic data, which is then stored in the memory in the defect data management server 103.

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Please replace paragraph [0094] with the following amended paragraph:

[0094] The classification results are stored in association with the defect coordinates 162, as shown in Fig. 11. In the coordinate consistency checking operation (b), [[The]]the defect data management server 103 reads into memory the electronic test results for the position corresponding to the defect coordinates stored in the storage device 108. Coordinate consistency checking is then performed to determine if there is a match with the defect coordinates. In the criticality calculation operation (c), the match rate between the defect coordinates and the electronic test results are tabulated for each of the image classification categories. A criticality rate KR, which is a value used for evaluation, is calculated as shown below. According to

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this definition, criticality increases as KR approaches 1, and criticality decreases as KR approaches 0.

$$KR=N_N/No \qquad \text{Expression (1)}$$

In expression (1), NN denotes the number of defects where the ~~fawt~~ fault position on the map of failed bits matches defect map coordinates. NO denotes the number of defects in the defect map.

Please replace paragraph [0104] with the following amended paragraph:

[0104] The method used to predict yield will be described. Defects can generally be classified as those generated in a concentrated manner and those generated randomly. In the present invention, the classification results for a set of defects selected by sampling can be used for overall predictions. This is suited for random defects. Yield from random defects can, for example, be calculated using the following equation.

$$Y=1-T/To \qquad \text{Expression (4)}$$

Here. Y represents the predicted yield. T represents the number of chips containing defects, and To represents the number of inspected chips. However, ~~sinee~~ since not all defects detected by the inspection device will necessarily be critical, criticality can be taken into account. Thus, expression (4) becomes the following equation.

$$Y_i =1 - KR_i * T_i / To \qquad \text{Expression (5)}$$

Here, Yi, represents the yield based on category i, KR1 represents the criticality of category i, Ti represents the number of chips containing defects classified as category I by the ADC device, and To represents the number of inspected chips.

Please replace paragraph [0106] with the following amended paragraph:

[0106] Next, a method for using the yield calculation results described above for fault prevention will be described with reference to Fig. 13 and Fig. 14. Once critical defects are discovered, it is important to ~~identffy~~ identify the causes and especially the processes during which the defects were generated. This allows the focus for critical defect prevention to be narrowed and ~~minimims~~ minimal defects by preventing critical defects from being generated. The coordinate consistency checking operation shown in Fig. 14 is used to identify the process in which a critical defect was generated. For example, defect inspections are performed more often in the processes prior to process m for individual wafers. If, for example, a dark-field inspection device capable of performing high-speed inspections is used for the inspection device 100, frequent defect inspections for processes prior to process in can be performed without delaying the processing of the product.

Please replace paragraph [0112] with the following amended paragraph:

[0112] Furthermore, the preparatory stage with the wafer A 121 can be ~~onutted~~ omitted and operations can be carried out solely for the active stage with the wafer B 122. If critical defects can be clearly determined from the detailed defect information, criticality can be assessed using the detailed defect information before the wafer reaches the electronic testing step. Defect analysis using the critical defect count can be performed as shown in Figs. 12(a) and 12(b).

Please replace paragraph [0115] with the following amended paragraph:

[0115] Another characteristic of the embodiment described above is that defect criticality, which was determined after completion of the wafer in the conventional technology, can be evaluated in a precise ~~maimer~~ manner in the visual inspection step, which is an intermediate process. Thus, analysis can be performed with higher priority being given to defects generated by yield-reducing factors that lead to high electronic criticality and high frequency of occurrence. This allows fault prevention measures to be started early.

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Please replace paragraph [0116] with the following amended paragraph:

[0116] Another characteristic of the embodiment described above is that a criticality rate can be quantitatively determined to indicate correlation between the detailed defect information and the actual electronic testing results as well as the degree of this correlation. As a result, yield, which is determined after wafer completion in the conventional technology, can be accurately determined at a stage before completion. This allows early evaluation of whether or not a required number of working products can be completed in time for a ~~sliipping~~ shipping date. By taking measures such as increasing production input, loss of sales opportunities can be prevented beforehand.

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